USE OF SOFTWARE AT OTHER PAGES BY 'OR'ING ADDRESSES

The SC/MP microprocessor fetches its first instruction from address location ØØØØ + 1 = ØØØ1. This means that if the instruction is in a ROM then this ROM must be located to begin at the first address the SC/MP will issue. (Actually for convenience such a ROM will often begin at ØØØØ rather than ØØØ1, with the first byte unused).

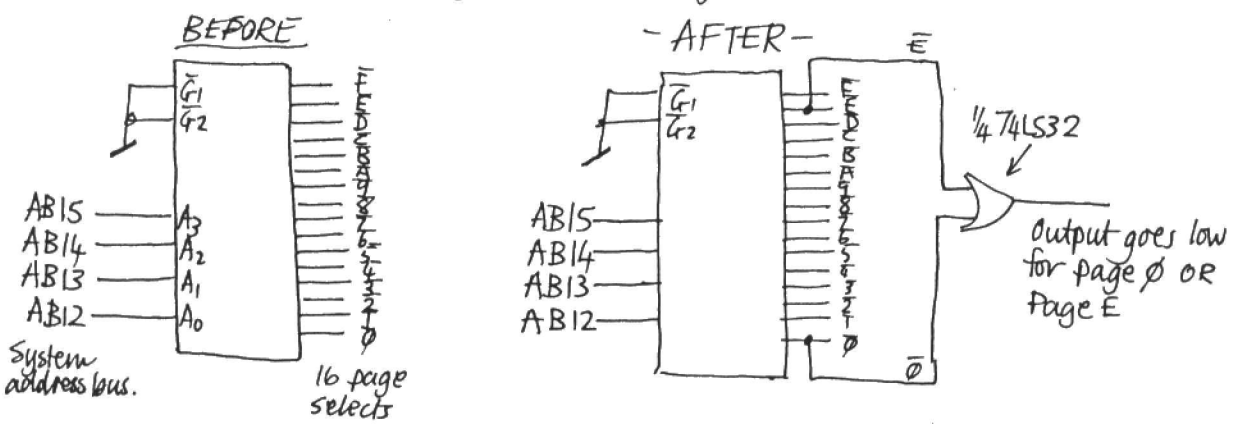
The user of a SC/MP microprocessor will often begin with the easy language NIBL, and will then later progress to machine code work as his needs and skills dictate. The memory map we suggest for various processors, including SC/MP, is described in our note AN-C23/1, and it will be seen that ØØØØ - ØFFF and EØØØ - E7FF have been chosen for firmware. The machine code monitor program is located at EØØØ in this new plan, and is reached from NIBL by typing 'LINK # EØØØ, carriage return', on the keyboard.

There is one user who is not catered for by this system, as so far described, and that is the person who wants to begin with machine code work and add NIBL later. A special version of the monitor program which begins at EØØØ could of course be written for ØØØØ onwards but this would have to be removed and modified if and when NIBL was added.

Therefore, it may be thought sensible to modify the hardware temporarily so that the EØØØ monitor etc. can be used as it stands. Since the first instruction is at EØØ1, and the SC/MP expects to find it at ØØØ1 then the address decoding must be modified so that the monitor can be reached at ØØØØ onwards OR EØØØ onwards.

Often in SC/MP systems, the 64K memory space is divided into 16 identical sections or 'pages'. Since 64K divided by 16 is 4K each of these pages is 4K in length. Using the nomenclature of 'pages' the requirement stated at the foot of the last page can be restated as follows: The monitor program should be reached on page 'E' or on page 'Ø'.

Since so many systems are unalike, it is not possible to be specific on the modifications needed to any individual set up, but in general whatever line used to select page Ø and whatever line used to select page E, should be 'OR'ed together using e.g. a 74LS32 'OR' gate. A typical system is indicated in the following diagrams - before and after the modification.



If for example a particular memory card was enabled previously by only a page Ē signal then the page Ē signal should be removed and the combine Ē OR Ø signal used instead. The memory devices on that card will then respond to an address on page Ē or page Ø, and so firmware which is written for page Ē can be used directly.

D.M.P. 15-12-80